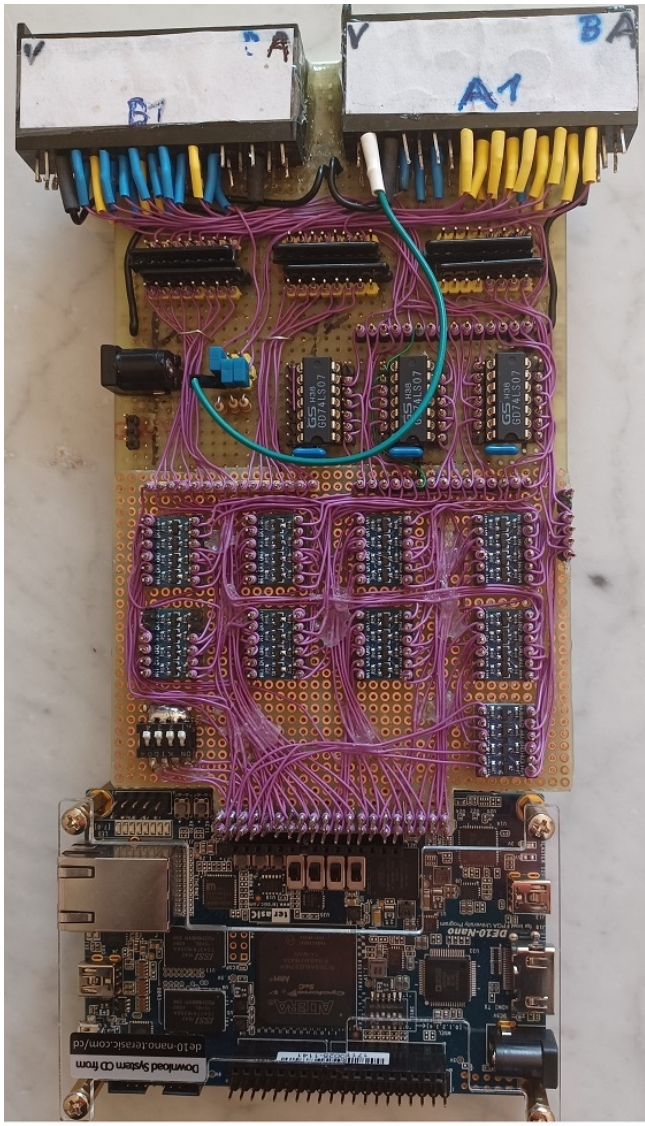
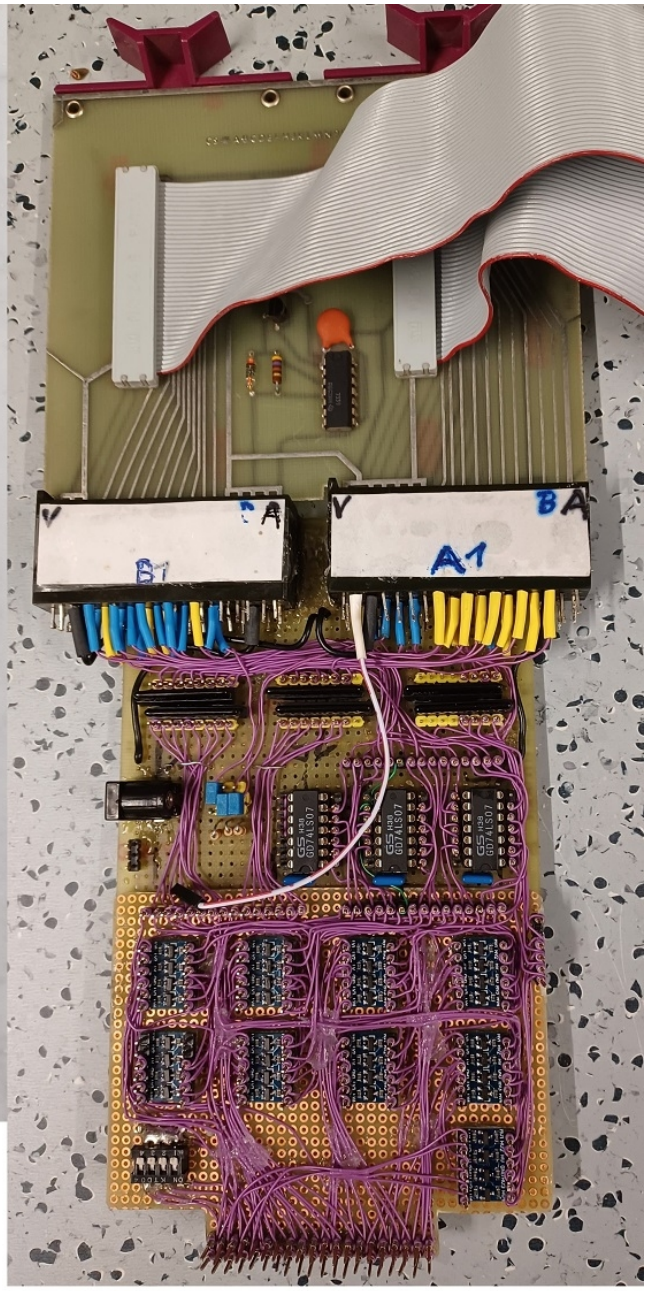
Development of the RK05 emulator

www.pdp11gy.com





Prototyp Interface board

Project start: January 2023

Also based on De10-Nano FPGA Board: http://pdp11gy.com/rk05_E.html
Reference projects: RL01/RL02 emulator: http://pdp11gy.com/rlstatusE.html
MFM-Disk emulator: http://pdp11gy.com/sddoneE.html
Open Source: https://github.com/pdp11gy/RK05-Disk-Emulator

Emulates up to 4 RK05 drives simultaneously
Supports mixed environment of emulated + real RK drives

Emulator Mode This mode supports a combination of real and emulated RK05 disk drives. Thus, it is possible to copy the data from a real disk drive into the emulated environment. However, there is still a computer system, e.g. a PDP-8 required. The interface is working in **Slave Mode** with the program **rkemulator**
Note: The Clone/Read mode = Master Mode is not implemented yet.

Data format (PDP-8 mode): The DEC RK05 disk drive did have a capacity of ~2.5 MB
The emulater is using the **.dec** format which contains all the sector information . Another disk format is the disk image structure **.dsk** which is used for CPU emulators like SIMH.
At write operation, the .dec file and the .dsk file will be written. At read operation, first try is to read the .dec file. If it does not exist, the .dsk file will be read.
RK05: .dsk file 3245728 byte .dec file = 3338752 byte
Assuming the 4 slide switches on the DE10-Nano board are in off position, the emulator will generate 4 emty .dsk and .dec file : rk05-0 to rk05-3

Open:

PDP-11 mode not implemented yet (16 sector /track)

PCB board not available yet, only one prototyp interface board

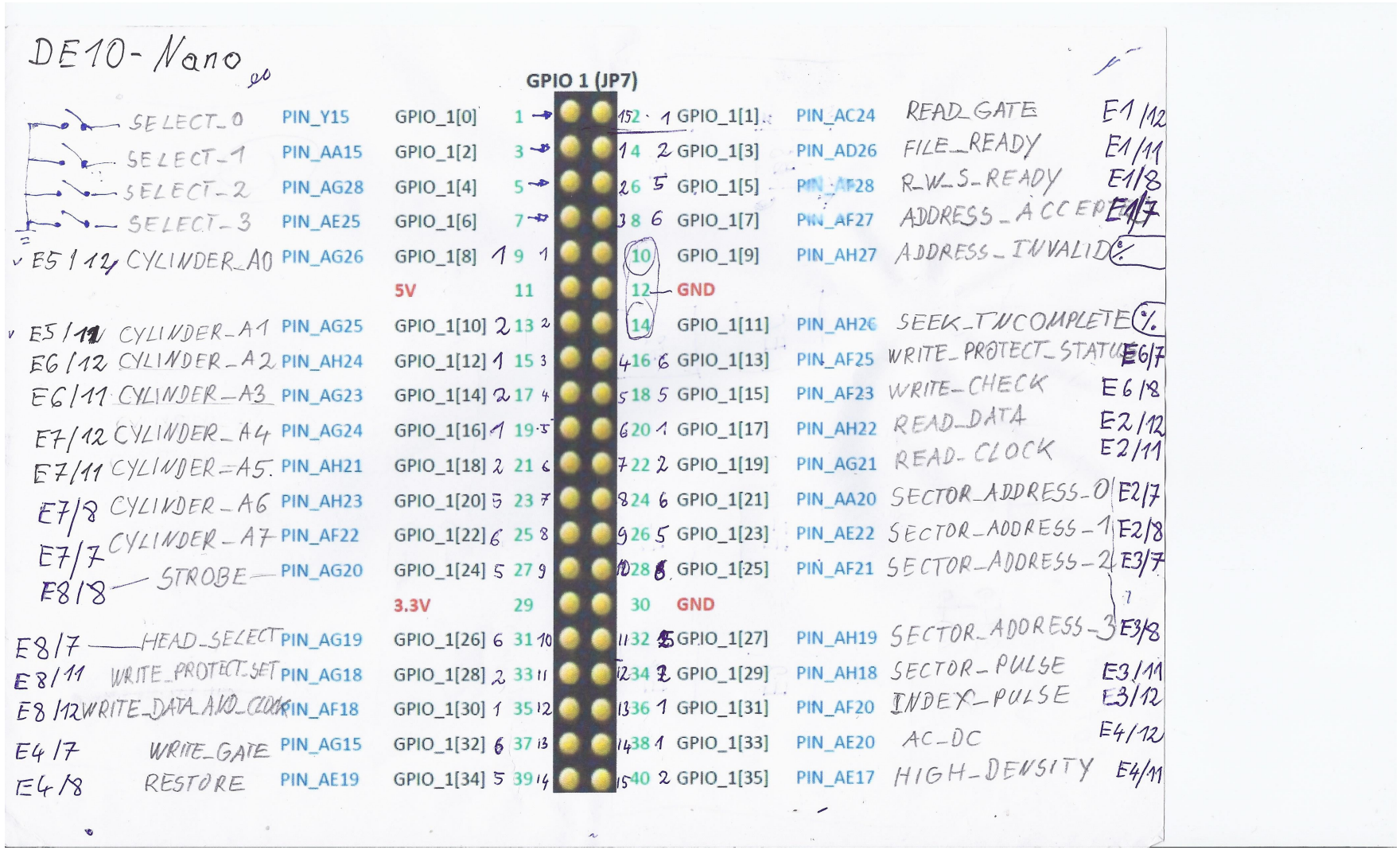
Test/verify environment not available, Hopefully starting June this year

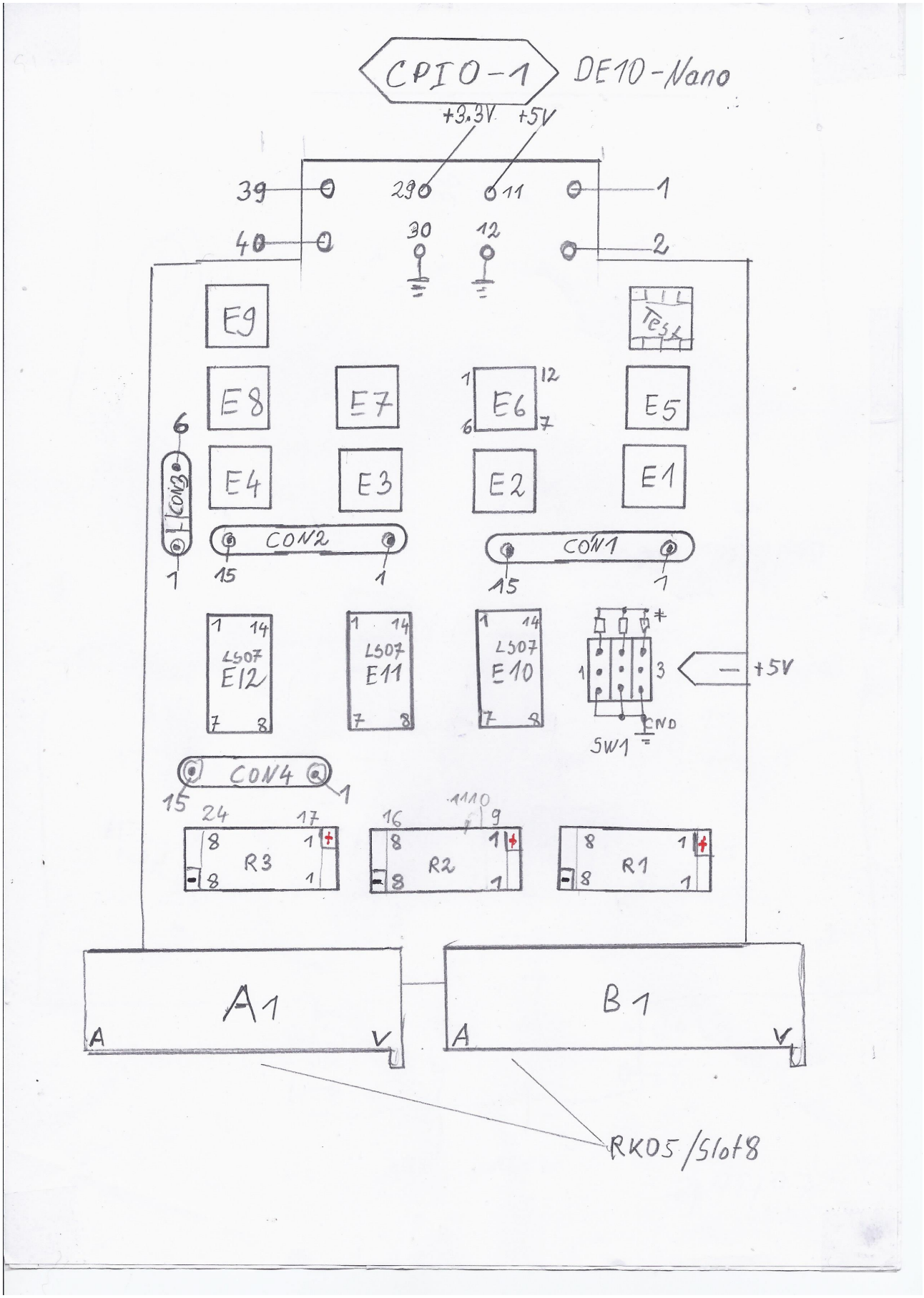
(Prototype) **Hardware**

The DE10-Nano board has 2 CPIO connectors available with 40 pins each, but 4 are always occupied. Thus 36 pins are freely available. However, the RK05 I/O bus consists of 38 signals, 20 for input and 18 for output. Result: 2 signals are too many. I solved this problem by not using unnecessary signals and permanently setting them to high or low. These signals are ADDRESS INVALID and SEEK INCOMPLETE and HIGH DENSITY(output).
One PIN is thus left and it will be used to select PDP-8 or PDP-11 mode.

A full, **ready for use** configured SD-card-image for the DE10-Nano Board is also available . Download the image from my homepage and copy it to the SD card with Win32DiskImager, for example. Login: root, PW: pdp11.
The associated directory is rk

Some hints: It is obvious that a RX01/RX02 emulator can be developed with relatively little effort. There are already such RX-floppy emulators, but not together with an RK05, RL01/02 and MFM-disk emulator. My plan is to develop a PCB board with level shifters for all 36 signals on the DE10-Nano board. Small interfaces can then be plugged onto this board for RL01/R02, MFM, RK05 and RX01/RX02 emulated disk drives.


DE10-Nano
GPIO 1 (JP7)
SELECT_0
SELECT_1
SELECT_2
SELECT_3
E5 / 12 CYLINDER_A0
E5 / 11 CYLINDER_A1
E6 / 12 CYLINDER_A2
E6 / 11 CYLINDER_A3
E7 / 12 CYLINDER_A4
E7 / 11 CYLINDER_A5
E7 / 8 CYLINDER_A6
E7 / 7 CYLINDER_A7
E8 / 8 STROBE
E8 / 7 HEAD_SELECT
E8 / 11 WRITE_PROTECT_SET
E8 / 12 WRITE_DATA_AND_CLOCK
E4 / 7 WRITE_GATE
E4 / 8 RESTORE
READ_GATE E1 / 12
FILE_READY E1 / 11
R_W_S_READY E1 / 8
ADDRESS_ACCEPT E1 / 7
ADDRESS_INVALID
SEEK_INCOMPLETE
WRITE_PROTECT_STATUS E6 / 7
WRITE_CHECK E6 / 8
READ_DATA E2 / 12
READ_CLOCK E2 / 11
SECTOR_ADDRESS_0 E2 / 7
SECTOR_ADDRESS_1 E2 / 8
SECTOR_ADDRESS_2 E3 / 7
SECTOR_ADDRESS_3 E3 / 8
SECTOR_PULSE E3 / 11
INDEX_PULSE E3 / 12
AC_DC E4 / 12
HIGH_DENSITY E4 / 11
PIN_Y15 GPIO_1[0] 1
PIN_AA15 GPIO_1[2] 3
PIN_AG28 GPIO_1[4] 5
PIN_AE25 GPIO_1[6] 7
PIN_AG26 GPIO_1[8] 9
5V 11
PIN_AG25 GPIO_1[10] 13
PIN_AH24 GPIO_1[12] 15
PIN_AG23 GPIO_1[14] 17
PIN_AG24 GPIO_1[16] 19
PIN_AH21 GPIO_1[18] 21
PIN_AH23 GPIO_1[20] 23
PIN_AF22 GPIO_1[22] 25
PIN_AG20 GPIO_1[24] 27
3.3V 29
PIN_AG19 GPIO_1[26] 31
PIN_AG18 GPIO_1[28] 33
PIN_AF18 GPIO_1[30] 35
PIN_AG15 GPIO_1[32] 37
PIN_AE19 GPIO_1[34] 39
2 GPIO_1[1] PIN_AC24
4 GPIO_1[3] PIN_AD26
6 GPIO_1[5] PIN_AF28
8 GPIO_1[7] PIN_AF27
10 GPIO_1[9] PIN_AH27
12 GND
14 GPIO_1[11] PIN_AH26
16 GPIO_1[13] PIN_AF25
18 GPIO_1[15] PIN_AF23
20 GPIO_1[17] PIN_AH22
22 GPIO_1[19] PIN_AG21
24 GPIO_1[21] PIN_AA20
26 GPIO_1[23] PIN_AE22
28 GPIO_1[25] PIN_AF21
30 GND
32 GPIO_1[27] PIN_AH19
34 GPIO_1[29] PIN_AH18
36 GPIO_1[31] PIN_AF20
38 GPIO_1[33] PIN_AE20
40 GPIO_1[35] PIN_AE17


GPIO-1
DE10-Nano
+3.3V
+5V
39
29
11
1
40
30
12
2
E9
Test
E8
E7
E6
E5
E4
E3
E2
E1
CON3
CON2
CON1
CON4
L507 E12
L507 E11
L507 E10
+5V
GND
SW1
R3
R2
R1
A1
B1
RK05/Slot8

INPUT Signals = TO FPGA ← Host

Signal NAME	FPGA/PIN	CON/PIN	R-Net	RK05/Slot8
SELECT 0	Y15/1	CON3/6	R3-5	A08-J2
SELECT 1	AA15/3	CON3/5	R3-6	A08-K2
SELECT 2	AG28/5	CON3/4	R3-7	A08-L2
SELECT 3	AE25/7	CON3/3	R3-8	A08-M2
CYLINDER ADDRESS 0	AG26/9	CON1/1	R1-1	A08-K1
CYLINDER ADDRESS 1	AG25/13	CON1/2	R1-2	A08-D1
CYLINDER ADDRESS 2	AH24/15	CON1/3	R1-3	A08-L1
CYLINDER ADDRESS 3	AH23/17	CON1/4	R1-4	A08-C1
CYLINDER ADDRESS 4	AG24/19	CON1/5	R1-5	A08-F1
CYLINDER ADDRESS 5	AH21/21	CON1/6	R1-6	A08-J1
CYLINDER ADDRESS 6	AH23/23	CON1/7	R1-7	A08-E1
CYLINDER ADDRESS 7	AF22/25	CON1/8	R1-8	A08-H1
STROBE	AG20/27	CON1/9	R2-1	B08-H1
HEAD SELECT	AG19/31	CON1/10	R2-2	B08-M2
WRITE PROTECT SET	AG18/33	CON1/11	R2-3	B08-R2
WRITE DATA AND CLOCK	AF18/35	CON1/12	R2-4	B08-F2
WRITE GATE	AG15/37	CON1/13	R2-5	B08-L2
RESTORE	AE19/39	CON1/14	R2-6	B08-M1
READ GATE	AC24/2	CON1/15	R2-7	B08-R1

Termination, all input signals @ CON3 and CON1

!50 Ohm to +5 V
330 Ohm to GRND

OUTPUT Signals FROM FPGA → Host

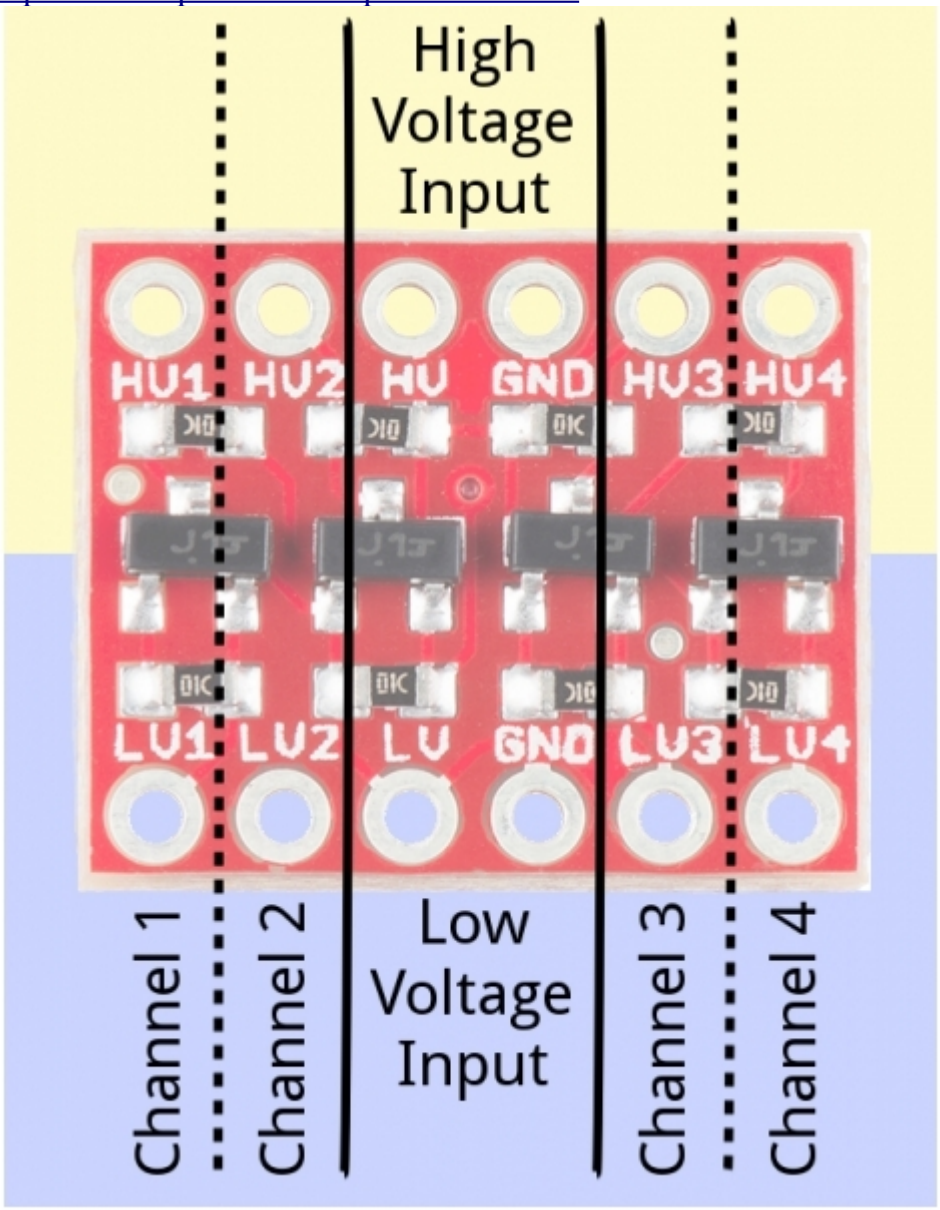
Signal NAME	FPGA/PIN	CON/PIN	E10-E11	RK05/Slot8
FILE READY	AD26/4	CON2/1	E10-5/6	B08-N1
R/W/S READY	AF28/6	CON2/2	E10-3/4	A08-H2
ADDRESS ACCEPTED	AF27/8	CON2/3	E10-1/2	A08-R2
(ADDRESS INVALID)	AH27/10	%	%	*(A08-T2)
(SEEK INCOMPLETE)	AH26/14	%	%	*(A08-S2)
WRITE PROTECT STATUS	AF25/16	CON2/4	E11-13/14	B08-P1
WRITE CHECK	AF23/18	CON2/5	E11-11/10	B08-K1
READ DATA	AH22/20	CON2/6	R11-9/8	B08-S2
READ_CLOCK	AG21/22	CON2/7	E11-5/6	B08-S1
SECTOR ADDRESS 0	AA20/24	CON2/8	E11-3/4	B08-L1
SECTOR ADDRESS 1	AE22/26	CON2/9	E11-1/2	A08-P2
SECTOR ADDRESS 2	AF21/28	CON2/10	E12-13/12	A08-K2
SECTOR ADDRESS 3	AH19/32	CON2/11	E12-11/10	A08-J1
SECTOR PULSE	AH18/34	CON2/12	E12-9/8	A08-N2
INDEX PULSE	AF20/36	CON2/13	E12-5/6	A08-M1
DC-LOW	AE20/38	CON2/14	E12-3/4	A08-F2
AC-LOW	AE17/40	CON2/15	E12-1/2	A08F1

Not connected FPGA PIN‘s :

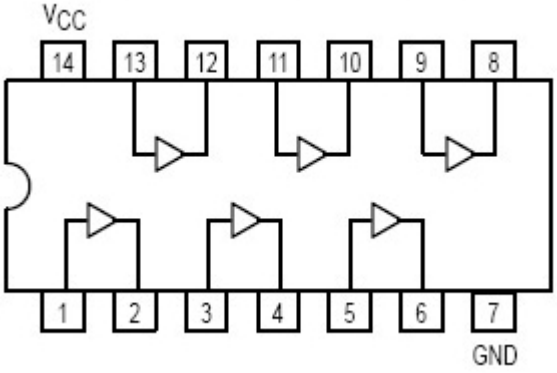
*ADDRESS INVALID - AH27/10 dropped → SW1/1 A08-T2 HIGH
*SEEK INCOMPLETE – AH26/14 dropped → SW1/2 A08-R2 HIGH
HIGH DENSITY → SW1/3 B08-P2 LOW

Used Chips:

https://www.sparkfun.com/products/12009



SN74LS07 Hex Buffers and Drivers With Open-Collector



It's just an idea , open but possible: attached RX01/RX02 interface.